

REMARKS

Objection to the Drawings

In the Office Action, the Examiner objects to the drawings under 37 CFR 1.83(a), stating:

The drawings must show every feature of the invention specified in the claims. Therefore, the details of "an N-to-M multiplexer comprising ... N control terminals coupled to the N output terminals of the first bi-directional shift register" must be shown or the features(s) canceled from the claims(s). No new matter should be entered. (emphasis original)

Applicants respectfully traverse this objection, on the grounds that the cited feature is already shown in the drawings. Claim 21 (the claim including the cited feature) reads as follows:

21. A multiplexer circuit, comprising:  
    N data input terminals, wherein N is an integer;  
    an output terminal;  
    a first bi-directional shift register comprising N bits and N output terminals, wherein exactly one of the N bits has a first token value;  
    an N-to-M multiplexer comprising N data input terminals coupled to the N data input terminals of the multiplexer circuit, N control terminals coupled to the N output terminals of the first bi-directional shift register, and M output terminals, wherein M is an integer less than N;  
    a second bi-directional shift register comprising M bits and M output terminals, wherein exactly one of the M bits has a second token value; and  
    an M-to-1 multiplexer comprising M data input terminals coupled to the M data output terminals of the N-to-M multiplexer, M control terminals coupled to the M output terminals of the second bi-directional shift register, and an output terminal coupled to the output terminal of the multiplexer circuit.

This claim reads on the embodiment of Figs. 4-12, for example, as follows. The "multiplexer circuit" corresponds to element 402, the bi-directional shift register/multiplexer shown in Figs. 4-6. The "N data input terminals" are labeled CLK0-CLKn in Fig. 4, and CLK0-CLK15 in Figs. 5 and 6. Thus, in the exemplary embodiment illustrated in the figures, N is sixteen.



The "output terminal" of the multiplexer circuit is labeled SEL\_CLK in Figs. 4-6.

The "first bi-directional shift register" is included, for example, in elements MA\_0 through MA\_15 of Fig. 6, as illustrated in Figs. 7-9. The "first bi-directional shift register" includes, for example, one instantiation of elements 701 and 702 in Figs. 7 (the "set bit"), and fifteen instantiations of elements 801 and 802 in Fig. 8 (the "reset bit"), as described in the specification at paragraphs [0044]-[0045] and as shown in Fig. 6. The N output terminals of the "first bi-directional shift register" are the N "Q" output terminals of the corresponding flip-flops 702, 802.

The "N-to-M multiplexer" is also included, for example, in elements MA\_0 through MA\_15 of Fig. 6, as illustrated in Figs. 7-8. The "N-to-M multiplexer" includes, for example, one instantiation of tristate buffer 703 in Fig. 7 and fifteen instantiations of tristate buffer 803 in Fig. 8. The N (16) control terminals of the "N-to-M multiplexer" are labeled "E" in Figs. 7 and 8, indicating that each control terminal enables the corresponding tristate buffer 703/803. Each control terminal "E" of the "N-to-M multiplexer" is coupled to a corresponding "Q" output terminal of a flip-flop 702, 703, i.e., to a corresponding output terminal of the "first bi-directional shift register". Thus, the "N control terminals coupled to the N output terminals of the first bi-directional shift register" are already illustrated.

The "second bi-directional shift register" and the "M-to-1 multiplexer" are included, for example, in the remaining elements MB\_0 through MB\_7, MC\_0 through MC\_3, MD\_0 and MD\_1 of Fig. 6, which can be implemented, for example, in a similar fashion to the "first bi-directional shift register" and "N-to-M multiplexer". Thus, the "M control terminals coupled to the M output terminals of the second bi-directional shift register" are also illustrated in Figs. 7 and 8.



Therefore, the figures do illustrate the element of Claim 21 to which the Examiner objected, and this objection is overcome. Hence, Applicants do not amend the figures at this time, and amended drawings are not included herewith.

#### Objections to the Specification

Applicants have amended paragraph [0059] to correct an erroneous reference numeral, as required by the Office Action. This amendment merely brings the specification into conformance with Figs. 10 and 12. Therefore, no new matter is added. Applicants thank the Examiner for detecting this error and allowing this opportunity for Applicants to correct the error.

The specification is further objected to as failing to provide proper antecedent basis for the claimed subject matter, the Office Action stating:

Correction of the following is required: the recited limitation "an N-to-M multiplexer comprising ... N control terminals coupled to the N output terminals of the first bi-directional shift register", in claim 21, is not supported either by the disclosure or the drawings. There is insufficient antecedent basis for this limitation in the claim. (emphasis original)

Applicants respectfully traverse this objection. Sufficient antecedent basis is supplied both in the drawings (e.g., Figs. 4-9) and the specification (e.g., the paragraphs describing these figures). Applicants respectfully refer the Examiner to the explanation of how the elements of Claim 21 relate to the figures, given above in regard to the objection to the drawings. Therefore, this objection is overcome.



Summary of Claim Status

Claims 3-7, 10-14, 16-18, and 20-24 are pending in the present application after entry of the present amendment. Claims 1, 2, 8, 9, 15, 19, and 21-24 are rejected for the reasons discussed below. Applicants have canceled Claims 1, 2, 8, 9, 15, and 19, thereby rendering the rejection of these claims moot.

Claims 3-7, 10-14, 16-18, and 20 are objected to as depending from a rejected base claim, but would be allowable if properly rewritten in independent form. Applicants thank the Examiner for this acknowledgement of patentable subject matter.

Applicants request the favorable reconsideration of the claims and withdrawal of the pending rejections and objections, in view of the present amendment and in light of the following remarks.

Rejections Under 35 USC 112

Claims 21-24 are rejected as being indefinite under 35 USC 112, second paragraph, the Office Action stating:

Claim 21 is indefinite because of the limitation "an N-to-M multiplexer comprising N data input terminals coupled to the N data input terminals of the multiplexer circuit, N control terminals coupled to the N output terminals of the first bi-directional shift register" on lines 7-1 [sic, lines 7-10]. It is unclear because it cannot be determined what kind of structural cooperative relationships of those elements is being claimed here.

Applicants respectfully traverse this rejection.

Applicants disagree with the statement that "it cannot be determined what kind of structural cooperative relationships of those elements is being claimed here." On the contrary, Applicants have clearly demonstrated above an exemplary interpretation of these elements, and how the elements are illustrated and described in the specification and figures as filed. Applicants respectfully refer the Examiner to the explanation of how the elements of Claim 21 relate to the figures, given above in regard to the objection to the drawings.



Therefore, Applicants believe the language of Claim 21 to be proper and definite. Claims 22-24 are rejected due to their dependency from Claim 21. Hence, Claims 22-24 are also believed allowable over the 35 USC 112 rejection.

Rejections Under 35 USC 102(b)

Claims 1, 2, 8, 9, 15, and 19 are rejected as being anticipated by Farwell (U.S. Patent No. 5,580,445). Applicants have cancelled Claims 1, 2, 8, 9, 15, and 19, thereby rendering this rejection moot.

Objections to the Claims

Claims 3-7, 10-14, 16-18, and 20 are objected to as being dependent from a rejected base claim, but otherwise allowable. Applicants have amended Claims 3, 6, 10, 13, 16, 18, and 20 to include the limitations of the corresponding base claims and any intervening claims. Claims 4, 5, 7, 11, 12, 14, and 17 depend from these amended claims. Therefore, Claims 3-7, 10-14, 16-18, and 20 are allowable as amended.

Please note that the amendments to Claims 3, 6, 10, 13, 16, 18, and 20 merely incorporate limitations previously included in parent claims. Therefore, these amendments are not narrowing and are not made for the purpose of patentability or avoiding the prior art.

Conclusion

No new matter has been introduced by any of the above amendments. All claims should now be in condition for allowance and a Notice of Allowance is respectfully requested. If any action other than allowance is contemplated by the

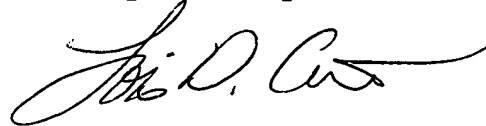


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Examiner, the Examiner is respectfully requested to telephone Applicant's agent, Lois D. Cartier, at 720-652-3733.

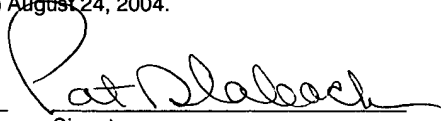
Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on August 24, 2004.

Pat Slaback  
Name

  
Signature